second rising edge being one period behind said first rising edge, wherein the delaying, phase-detecting and adjusting is irrespective of the comparison when starting the delay adjustment.

A copy of the marked up amended claims is attached to this response showing the changes as set forth in amended 37 C.F.R. § 1.121.

REMARKS

Claims 1-8 are pending in this application. By this Amendment, claims 1 and 3-7 are amended to more particularly point out and clarify the "delaying" and "initiation period" aspect of the invention. No new matter is added. This Amendment is submitted as a full and complete response to the outstanding Office Action.

Applicant respectfully submits that entry of this Amendment is proper under 37 C.F.R. § 1.116 since this Amendment: (a) does not raise any new issue regarding further search and/or consideration since the amended claim language only clarifies subject matter already presented in the Applicant's previous response(s); (b) does not present any additional claims; and (c) places the application in better form for appeal, should an appeal be necessary. Entry of the Amendment is thus respectfully requested. Accordingly, reconsideration of the application in view of the following remarks is respectfully requested.

MATTERS OF FORM

The Office Action objects to claim 6 for a typographical error. Applicant has amended claim 6 to obviate the objection. Accordingly, Applicant respectfully requests the withdrawal of the objection to claim 6.

The Office Action rejects claims 1-4 and 6-8 under 35 U.S.C. § 112, first paragraph.

Specifically, the Office Action asserts that the recitation of "delaying is irrespective of the comparison during an initiation period" in the claims is not described in the originally-filed specification.

Applicant has amended the claims to recite "when starting the delay time adjustment" to clarify the rejected claim language. The amended language is supported in the Applicant's specification on page 13, lines 22-35 and on page 15, lines 29-35, for example. The language in the specification recites features relating to and similar to the rejected language. As stated in MPEP § 2163.02, the subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement.

For example, as explained in the Applicant's specification, the delay time adjustment period may be defined as a period from the cancellation of the power-on reset signal until the output signal of the phase comparator changes from high (delay increase) to low (delay decrease) for the first time. Further, the delay time adjustment period may also be defined as a period from the cancellation of the power-on reset signal to the time when the phases of the target clock and the delay match each other for the first time. Additionally, the delay time adjustment period may be defined as a period, in a case where the rising edge of the delay clock (dclk) at VD = Min. is behind the rising edge of the target clock (tclk).

In view of the clear teaching of the Applicant's specification, Applicant respectfully submits that the specification supports the claimed language. Therefore, for at least the above reasons, Applicant respectfully requests the withdrawal of the rejection under 35 U.S.C. § 112, first paragraph.

CLAIMS 1-8 CONTAIN PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1-8 under 35 U.S.C. § 102(e) over Lu (U.S. Patent No. 6,100,735). This rejection is respectfully traversed.

Applicant's independent claim 1 recites a delay time adjusting method of adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other, based on a comparison between phases of the input signal and the output signal, the method comprising the steps of increasing the delay time to adjust the phase of the output signal irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 3 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the method comprising the step of adjusting the delay time so that, when a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein the adjusting of the delay is irrespective of the comparison when starting the adjusting of the delay.

Applicant's independent claim 4 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first

periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the method comprising, a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of the input first periodic signal, and a second step of increasing the delay time to adjust the phase of the output second periodic signal so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge in said first step, the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, wherein the judging and delaying is irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 5 recites a delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other between phases based on a comparison of the input signal and said output signal, the circuit comprising, detecting means for detecting a phase difference between the phase of the input signal and the phase of the output signal, and delaying means for increasing a delay time of the phase of the output signal irrespective of the detection of phase difference when starting the delay time adjustment until the phase difference becomes N periods, where N is an integer other than zero.

Applicant's independent claim 6 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a

comparison between phases of the input first periodic signal and the input second periodic signal, the circuit comprising, judging means for judging whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, and delaying means for adjusting the delay time so that, when the phase of the predetermined rising edge of the output second periodic signal is judged to be behind the phase of the predetermined rising edge of the input first periodic signal by the judging means, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein the judging and delaying is irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 7 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the circuit comprising, delaying means for delaying the input first periodic signal so as to generate the output second periodic signal, phase-detecting means for detecting whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a first rising edge of the input first periodic signal; and adjusting means for controlling the delaying means so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge by the phase-detecting means, the delaying means delays the phase of the output

second periodic signal until the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, wherein the delaying, phase-detecting and adjusting is irrespective of the comparison when starting the delay adjustment.

Lu discloses a delay time adjusting method utilizing a coarse DLL and a fine DLL to generate incremental delay adjustments. As illustrated in Figs. 7A-C of Lu, overadjustment of the phase may occur as a multiple of integral periods. Lu solves this problem by devising a dual-pulse stimulus to the DLL during initialization to prevent double-delay operation. See Fig. 8 and col. 8, lines 37-40, for example. A pair of pulses and a 7-blanking period repeats. The rising edge of the first pulse arms the DLL's phase detector and propagates through the series of delay buffers, allowing phase comparison to occur for the second pulse. The DLL can only phase compare during the second pulse. The DLL is modified so that phase comparison can only occur when the phase detector is armed by the first pulse. The DLL becomes stable at a total delay of 1ICLK period with the bias voltage properly set. See col. 8, lines 46-66, for example. Lu also discloses an arming circuit for the phase detector in the coarse DLL. The arming input prevents phase comparison when low, but allows phase detection when high. See col. 9, lines 12-13 and 19-20, for example.

Therefore, it is readily apparent from the above that Lu does not perform a phase comparison or delay adjustment during the "start up" period and thus does not disclose or suggest increasing the delay time to adjust the phase when starting the delay time adjustment.

Accordingly, Applicant respectfully submits that Lu does not disclose or suggest all the claimed features of Applicant's invention. Claims 2 and 8 depend from claims 1 and 7, respectively. Therefore, for at least the above reasons, Applicant respectfully requests the withdrawal of the rejection of claims 1-8 under 35 U.S.C. § 102(e).

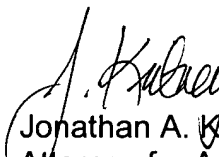
CONCLUSION

In view of the above remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance is earnestly solicited. Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 100353-00039.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



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Enclosures: Marked-Up Copy of Amended Claims

MARKED-UP COPY OF AMENDED CLAIMS

1. (Twice Amended) A delay time adjusting method of adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other, based on a comparison between phases of said input signal and said output signal, the method comprising the steps of:

[delaying] increasing the delay time to adjust said phase of said output signal irrespective of said comparison [during an initiation period] when starting the delay time adjustment.

3. (Twice Amended) A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the method comprising the step of:

adjusting said delay time so that, when a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal, wherein the adjusting of said delay is irrespective of said comparison [during an initiation period] when starting the adjusting of said delay.

4. (Twice Amended) A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison

between phases of said input first periodic signal and said input second periodic signal, the method comprising:

a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

a second step of [delaying] increasing the delay time to adjust said phase of said output second periodic signal so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge in said first step, said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal [march] match each other, the second rising edge being one period behind said first rising edge, wherein the judging and delaying is irrespective of said comparison [during an initiation period] when starting the delay time adjustment.

5. (Twice Amended) A delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of said input signal and a phase of an output signal match each other between phases based on a comparison of said input signal and said output signal, the circuit comprising:

detecting means for detecting a phase difference between said phase of said input signal and said phase of said output signal; and

delaying means for [delaying] increasing a delay time of said phase of said output signal irrespective of said detection of phase difference when starting the delay time adjustment until said phase difference becomes N periods, where N is an integer other than zero.

6. (Twice Amended) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a [phse] phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the circuit comprising:

judging means for judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal; and

delaying means for adjusting said delay time so that, when said phase of said predetermined rising edge of said output second periodic signal is judged to be behind said phase of said predetermined rising edge of said input first periodic signal by said judging means, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal, wherein the judging and delaying is irrespective of said comparison [during an initiation period] when starting the delay time adjustment.

7. (Twice Amended) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the circuit comprising:

delaying means for delaying said input first periodic signal so as to generate said output second periodic signal;

phase-detecting means for detecting whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

adjusting means for controlling said delaying means so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge by said phase-detecting means, said delaying means delays said phase of said output second periodic signal until said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge, wherein the delaying, phase-detecting and adjusting is irrespective of the comparison [during an initiation period] when starting the delay adjustment.